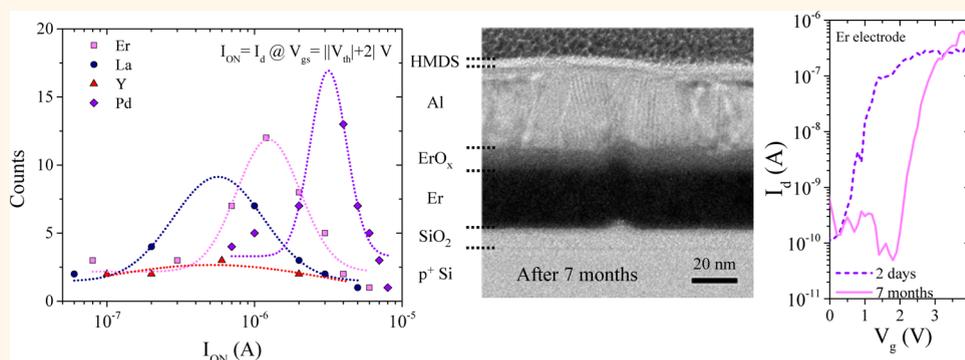# High-Performance Air-Stable n-Type Carbon Nanotube Transistors with Erbium Contacts

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ABSTRACT

So far, realization of reproducible n-type carbon nanotube (CNT) transistors suitable for integrated digital applications has been a difficult task. In this work, hundreds of n-type CNT transistors from three different low work function metals—erbium, lanthanum, and yttrium—are studied and benchmarked against p-type devices with palladium contacts. The crucial role of metal type and deposition conditions is elucidated with respect to overall yield and performance of the n-type devices. It is found that high oxidation rates and sensitivity to deposition conditions are the major causes for the lower yield and large variation in performance of n-type CNT devices with low work function metal contacts. Considerable improvement in device yield is attained using erbium contacts evaporated at high deposition rates. Furthermore, the air-stability of our n-type transistors is studied in light of the extreme sensitivity of these metals to oxidation.

KEYWORDS: carbon nanotube · n-type transistors · low work function metals · device yield

Over the past few decades, the continued down-scaling of the physical dimensions of silicon field-effect transistors (FETs) has been the main drive for achieving higher device density while improving the transistor performance in complementary metal–oxide–semiconductor (CMOS) circuits. One of the principle benefits of the conventional scaling trend, namely, reducing the power consumption per computation, has diminished in recent years. In particular, power management is increasingly becoming a major challenge because of the inability to further decrease the operating voltage without compromising the performance of silicon FETs.

Incorporation of alternative channel materials with superior carrier transport properties, as presently conceived, is a favorable strategy for the semiconductor industry to complement or replace silicon FETs. Among the promising candidates, carbon nanotubes (CNTs) are predicted to offer the most energy-efficient solution for computation compared with other channel materials,[1] owing to their unique properties such as ultrathin body and ballistic carrier transport in the channel.[2,3] Remarkable progress in addressing some of the key practical hurdles associated with CNTFETs has brought renewed attention to the field. Most notably, experimental reports showing significant placement control for solution-based CNTs[4] and high-performance CNT transistors with channel lengths smaller than 10 nm[5] mark two of the most recent stepping stones for enabling a CNT-based technology for logic applications.

p-Channel CNTFETs (pFETs) are routinely fabricated using high work function metals such as palladium (Pd) with superb performance and high device yield.[3,6] However, the realization of a concurrently reproducible and air-stable process for making n-channel CNTFETs (nFETs) with commensurate performance and device yield to pFETs is challenging. Chemical[7,8] and electrostatic[9−11] doping schemes that provide excess positive charges in the vicinity of the source contact were used to facilitate electron tunneling through the Schottky barrier into the channel simply by manipulating the width of the energy barrier. Despite successful demonstrations of nFET operation, the stochastic nature of the process-induced positive charges near the source contact can lead to unacceptable device variability and reliability issues when exploiting such methods in highly integrated digital applications. On the other hand, recent reports demonstrated the feasibility of low work function metals such as yttrium[12] (Y, $\Phi_M = 3.1$ eV), scandium[13] (Sc, $\Phi_M = 3.5$ eV), and gadolinium[14] (Gd, $\Phi_M = 3.1$ eV) contacts to permit nFET operation by direct electron injection into the conduction band. The nFETs made from Sc and Y contacts were shown to exhibit performance on par with Pd-contacted pFETs. Moreover, these low work function metal contacts were implemented to experimentally demonstrate various full CMOS CNT-based logic gates.[14−16] Despite these demonstrations of nFETs, a systematic study to investigate the impact of various low work function metals on the device performance, yield, and air-stability is still lacking in the literature.

In this Article, we present a thorough experimental study of device yield and performance for several low work function metal contacts, including erbium (Er, $\Phi_M = 3.0$ eV), lanthanum (La, $\Phi_M = 3.5$ eV), and Yttrium ($Y = 3.1$ eV). Extensive material characterizations are performed to study and correlate the oxidation properties of these metals with the device characteristics. Our results for nFETs with different metal electrodes indicate the ability to improve the device yield and performance by appropriate metal selection and optimization of deposition conditions. In addition, the stability of the nFET electrical characteristics was examined upon storage in ambient air, a crucial consideration from a technological standpoint, as the low work function metals are prone to rapid oxidation. Proper passivation of Er electrodes simply by a monolayer of hydrophobic polymer is shown to provide marked improvement of the device durability after nearly seven months' storage in air.

RESULTS AND DISCUSSION

Material, Device Yield, and Air-Stability Studies. In Schottky-barrier CNTFETs, tunneling through the barrier at the source/channel interface plays a crucial role in determining carrier injection into the channel.[17] Furthermore,

the symmetric energy band structure of CNTs is expected to lead to comparable performance for n- and p-FETs with similar Schottky barriers for both electron and hole carriers. Note that the Schottky barrier height depends not only on the work functions of the metal and the CNT but also on the interface properties and the extent of coupling between the metal contact and the CNT. Numerous reports investigating the overall performance of pFETs using various high work function metals underscore the importance of the metal/CNT interface.[6,18] Furthermore, despite the very similar work function of Sc, Y, and Gd metals, the reported electrical characteristics of the resulting nFETs are different.[12−14] For this reason, we examine the suitability of Er and La metals, considering their proper work function and routine use in mainstream silicon manufacturing, for making nFETs. To provide a comparison with the previously reported choices, we additionally prepared devices with Y contacts, in light of its excellent reported device properties,[12] to establish a baseline.

Several chips were fabricated with different electrodes from Er, La, Y, and Pd metals to investigate device yield. Each chip has 768 potential CNTFETs with a printed channel length of 300 nm. A global back gate device structure, depicted in Figure 1a, was used in this study owing to its simplicity for device integration. Purified solution-based CNTs[19] with a diameter distribution of 1.4 ± 0.1 nm were dispersed on p+ silicon
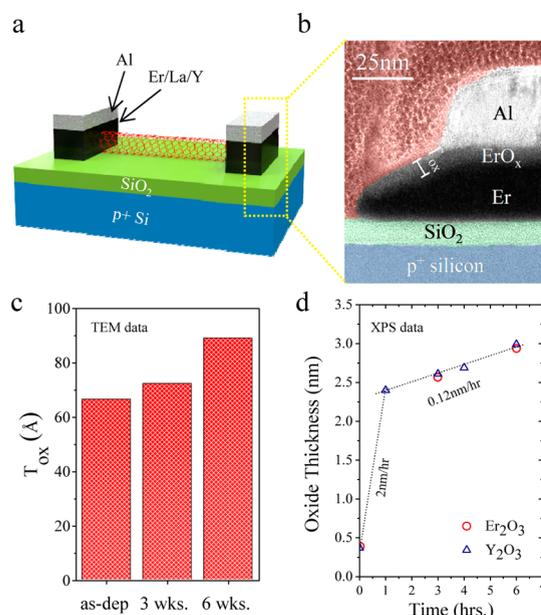

Figure 1. Material characterization of the low work function electrodes. (a) Schematic illustration of a bottom gate CNT nFET used in this study. **(b)** Representative cross-sectional TEM image of an as-deposited Er electrode capped with Al. **(c)** Plot of the ErOx thickness in the nonprotected region (T_{ox}) of the TEM specimen as a function of time, indicating the non-self-limiting nature of the oxide. **(d)** In situ XPS study of the blanket low work function metals under UHV conditions reveals the extreme sensitivity of these metals to oxidation.

substrates capped with 10 nm thermal SiO_2, followed by contact patterning using electron-beam lithography. Source and drain electrodes were then formed using a lift-off process. Because of the random distribution of the nanotubes on the surface, a large number of electrodes may not intercept a CNT (Figure S1 in the Supporting Information). Therefore, the chips were prepared using the same density CNT solution in order to obtain samples with a fairly consistent number of contacted nanotubes. Furthermore, the actual gate length of devices across a sample may slightly deviate from the printed length as a result of the random orientation of the nanotubes.

Figure 1b is a representative transmission electron microscopy (TEM) image of an as-deposited Er contact that was capped *in situ* with aluminum (Al). Surprisingly, the TEM study reveals the presence of an erbium oxide (ErO_x) interlayer formed under ultrahigh vacuum (UHV) conditions (4×10^{-9} Torr) during the brief pause between the Er and Al deposition steps. Note that the existence of such an unintended oxide interlayer can severely limit the extrinsic device performance because of the added series resistance. The TEM sample was then stored in ambient air for up to six weeks and imaged in the interim to monitor the evolution of the erbium oxide thickness in regions with and without the protective Al layer (Figure S2 in the Supporting Information). The progression of the oxidation front in the nonprotected region, measured from the TEM micrographs, is shown in Figure 1c. The finding of this study suggests that the oxidation process is not self-limiting at this metal thickness. On the other hand, the unchanged erbium oxide thickness underneath the Al layer confirms that the use of a capping layer effectively preserves the low work function metal electrode from oxidation.

To further investigate the oxidation properties of low work function metals, blanket films of Er and Y were prepared at 4×10^{-9} Torr and monitored *in situ* using X-ray photoelectron spectroscopy (XPS). The evolution of the oxide thickness is plotted in Figure 1d as a function of time for both the Y and Er films, extracted from the fitted curves to their corresponding XPS data (Figure S3 in the Supporting Information). The strong propensity of the low work function metals to rapidly oxidize, even under UHV conditions, is manifest in this plot. It is therefore essential to fully encapsulate the metal electrodes in the final device structure to prevent its oxidation, thus enabling air-stable nFETs.

In light of the oxidation properties of these metals under UHV conditions, it is important to consider the possibility of partial oxidation of the metal electrodes during the deposition process. To investigate this effect, several chips were prepared with various Er and Y thicknesses deposited at an extremely slow deposition rate of ~2.5 Å/min. The corresponding transfer characteristics of the resulting devices are
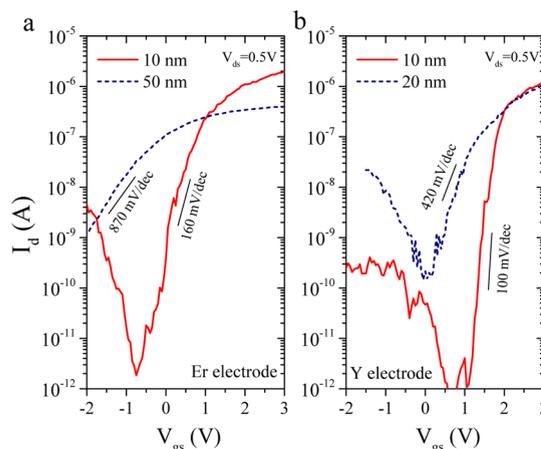

Figure 2. Effect of partial oxidation of the electrodes on device performance. Representative transfer characteristics of nFETs with "thin" and "thick" metal electrodes made from (a) Er and (b) Y deposited at an extremely slow deposition rate of 2.5 Å/min, subsequently capped with 30 nm Al. The device characteristics further degraded as the thickness of the metal electrode was increased.
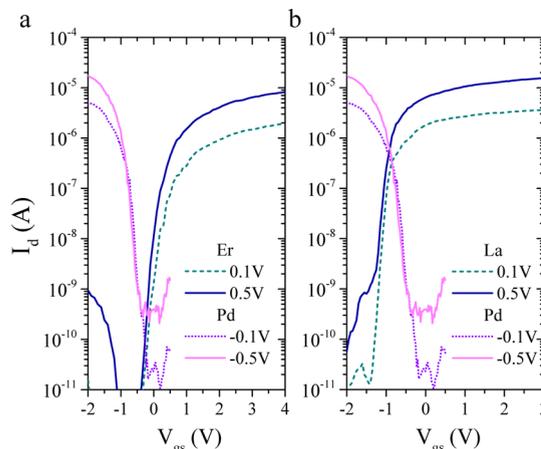

Figure 3. Impact of high deposition rate on device performance. Representative transfer characteristics of the "best" nFETs with (a) Er and (b) La electrodes evaporated at a deposition rate of 0.5−1 Å/s, exhibiting comparable performance to a representative "best" Pd-contacted pFET device.

plotted in Figure 2. It is evident from the data that the device characteristics further degraded as the contact layer thickness was increased, conceivably because of a higher degree of the metal contact oxidation. In addition, the device yield was plagued by the slow deposition rate, whereby only a handful of devices ($\leq$10 counts per chip) were found to exhibit an nFET-like behavior.

To alleviate the partial oxidation of the metal contact during the evaporation process, the deposition rates of the metal electrodes were increased to 0.5−1 Å/s. A pFET chip with Pd electrodes was also prepared for the purpose of device yield and performance comparisons. Figure 3a,b illustrate the transfer characteristics of representative "best" devices, in terms of the on current, with Er and La contacts, respectively. Each of the nFET
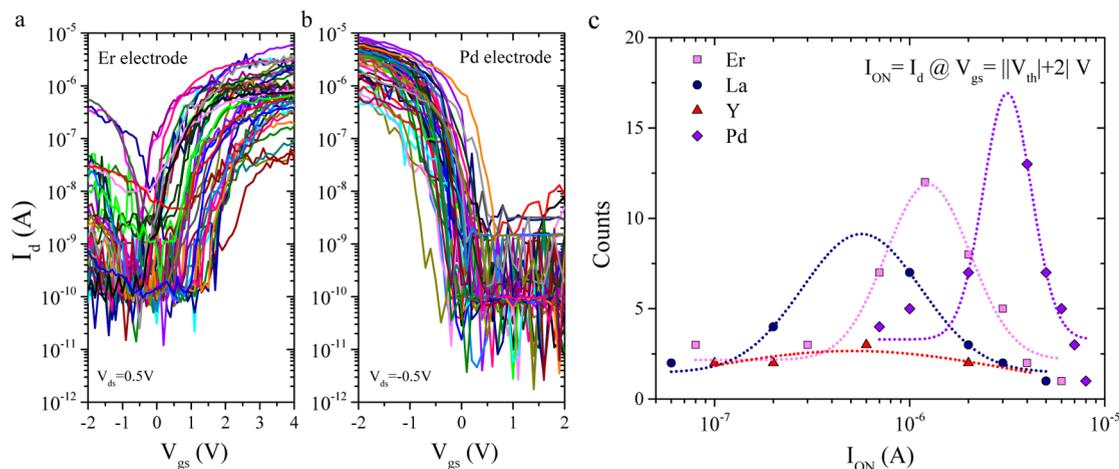
Figure 4. Device yield assessment. Transfer characteristics of CNT devices on two chips with (a) Er and (b) Pd contacts, showing comparable device count. (c) Comparison of I_{ON} distributions for chips with Er, La, Y, and Pd electrodes. I_{ON} was extracted for each chip from its corresponding $I_d - V_g$ curves, similar to the plots in (a) and (b).
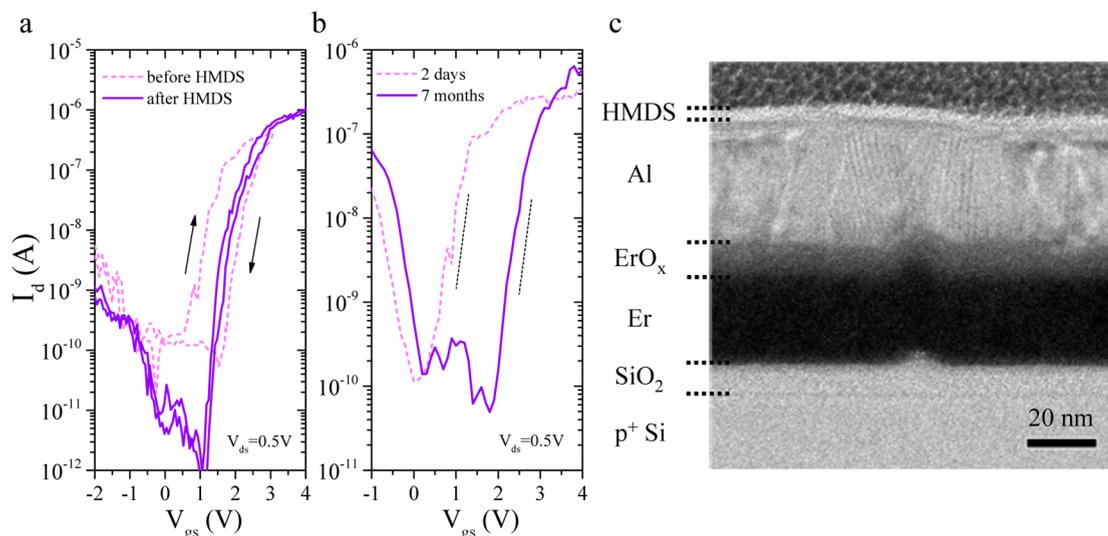

Figure 5. Device passivation study using self-assembled polymeric monolayer. (a) Reduction of hysteresis was achieved by HMDS deposition at 150 °C in a vacuum. (b) The electrical characteristics of the passivated nFETs remained stable upon storage in air, confirming the air-stability of Er-contacted devices. (c) Representative TEM image of an aged device, confirming the effectiveness of the HMDS seal in preventing further oxidation of the Er contact.

curves is overlaid on one of the "best" pFETs, demonstrating comparable device characteristics. The higher deposition rate was additionally found to result in remarkable improvement of the nFET device count.

To evaluate the overall device yield from different metal electrodes including Y, Er, La, and Pd, the transfer characteristics of devices were measured at $|V_{ds}| = 0.5$ V. Figure 4a,b show a side-by-side comparison of the $I_d - V_g$ curves for chips with Er and Pd contacts, exhibiting a comparable number of functional devices. The on current (I_{ON}) distribution for each chip was subsequently extracted from their corresponding $I_d - V_{gs}$ curves and plotted in Figure 4c. The distribution data elucidate the importance of the metal choice, in which the use of Er was shown to give rise to higher device count and tighter I_{ON} spread compared with La and Y.

It is notable that an identical protocol was used consistently for tube depositions in order to allow nearly similar CNT density on various samples. Nonetheless, the possible spatial variations in the tube density across each sample and conceivably the presence of devices with multiple CNTs may introduce a slight error in our device yield plot shown in Figure 4. Therefore, one straightforward approach to circumvent these potential sources of error in assessing the device yield is to simply use a placement technique for achieving tighter control over the spatial distribution of CNTs.

Hysteretic behavior of drain current and inconsistency of threshold voltage are among the practical challenges for utilizing CNTFETs in integrated digital applications. Various empirical studies on CNT pFETs suggest that surface charges from water molecules and

other volatile residual impurities residing on the tube surface are the primary origin of device variability.[20,21] In this study, we surprisingly observed that the nFET chips consistently demonstrate a noticeably larger degree of threshold voltage and I_{ON} variations compared to their pFET counterparts, evident from the data in Figure 4. We attribute this higher level of variability for nFETs to the inconsistency at the metal/CNT interfaces across a sample as a result of the extreme sensitivity of the low work function metals to oxidation.

Franklin *et al.* have recently reported that the variations of pFET device parameters can be diminished by thermal desorption of the volatile surface charges followed by the application of self-assembled hydrophobic monolayer polymers such as hexamethyldisiloxane (HMDS).[22] To investigate the benefits of this passivation scheme in mitigating the hysteresis window for the nFETs, HMDS was deposited on the nFET chips with Er and La contacts under ~1 Torr at 150 °C for 30 min. This experiment revealed the extreme thermal instability of the devices with La contacts, leading to the full oxidation of the La film. This was substantiated from the absence of functional devices on the chip after the HMDS treatment. However, we observed that the application of the hydrophobic monolayer to the surface of nFETs with Er contacts effectively reduces the hysteresis window, shown in Figure 5a. More importantly, it was found that the passivation of the nFETs with HMDS significantly improved the longevity of the devices upon storage in ambient air in excess of seven months, as evident from Figure 5b. Figure 5c illustrates the representative TEM image of an aged device with bundled

tubes, which was chosen to facilitate imaging, corroborating the effectiveness of the encapsulating layer in preventing the oxidation of the Er electrode. Although device passivation with HMDS is incompatible with the full CMOS process flow from the temperature stability standpoint, this study in essence indicates the prospects for realizing air-stable nFETs using low work function metal electrodes encapsulated by a hermetic seal.

CONCLUSIONS

In conclusion, we studied the impact of several low work function metals including Er, La, and Y on the overall device yield and performance of nFETs. Our findings suggest that a remarkable improvement in nFET device characteristics can be achieved employing Er contacts. Extensive material characterizations confirmed the susceptibility of these metals to rapid oxidation. The device yield and performance were consequently improved by mitigating the metal oxidation through controlling the process conditions, including the base pressure and the deposition rate. The formation of an undesirable erbium oxide interlayer was discerned between the metal electrode and the Al protective layer. The presence of a parasitic interlayer is expected to limit the extrinsic device performance by degrading the contact resistance. The electrical characteristics of nFET devices with Er electrodes were shown to remain stable upon storage in air by employing a hydrophobic polymer deposited at 150 °C. This encouraging result indicates the possibility of making air-stable nFETs from low work function metals for high-performance electronic applications.

METHODS

A 1 mg/mL solution of CNTs (Hanhwa Nanotech) in a 1% aqueous SDS (Sigma Aldrich) solution was prepared *via* sonication. The solution was then purified using a step gradient ultracentrifugation step.[20] Prior to CNT deposition, the CNT solution was diluted with a 1% sodium cholate solution (typically 1:20) and sonicated for 20 min. The CNTs were then dispersed on a p$^+$ silicon wafer capped with 10 nm of thermally grown SiO_2 by placing a few drops on the substrate and allowing it to stand for several minutes, followed by nitrogen blow drying. The substrate was then gently rinsed with methanol to remove excess surfactant. Source/drain electrodes were formed *via* metal lift-off in acetone at 70 °C. The electrical data shown in Figure 4 were measured in air. However, the remaining electrical measurements shown in other plots were made under vacuum.

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